

Fig 3.

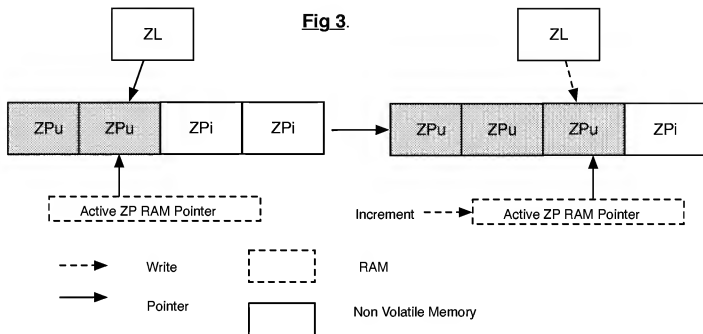
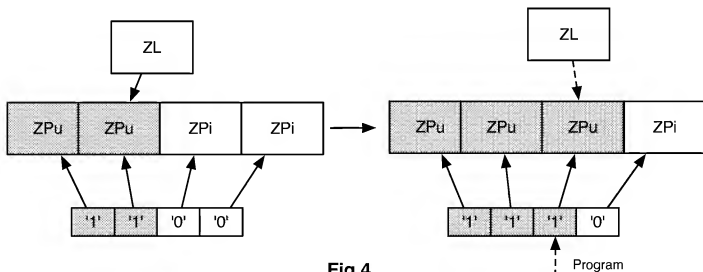


Fig 4.



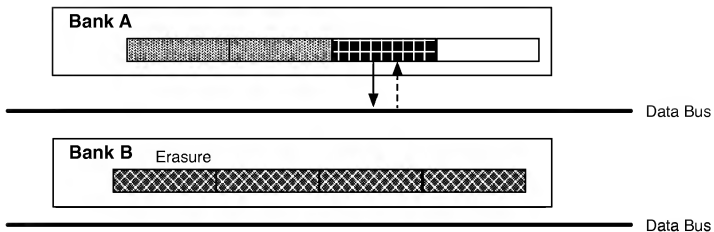


Fig. 7a

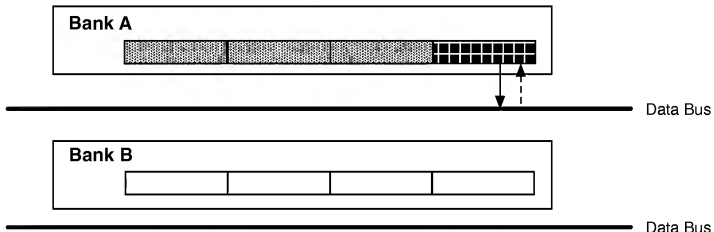


Fig. 7b

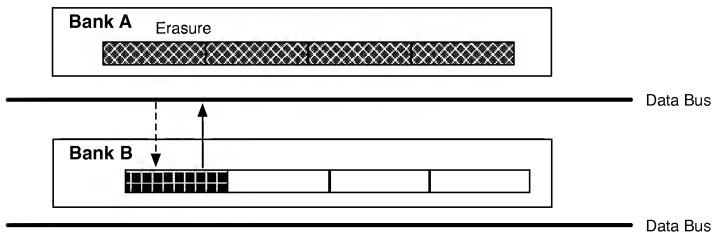
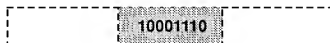
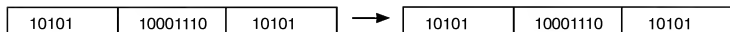


Fig. 7c



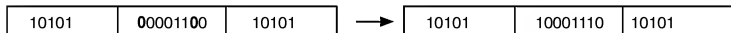
Value to be written in the logical area



ZPn

Fig 5a

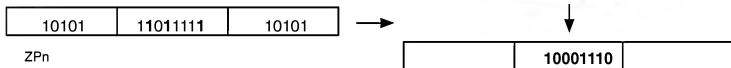
ZPn



ZPn

Fig 5b

ZPn



ZPn

Fig 5c

ZPn+1